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Short communication

Direct wafer bonding of Ga_2O_3–SiC at room temperature

Yang Xu[a,b,c], Fengwen Mu[a,*], Yinghui Wang[b,c,d], Dapeng Chen[b,c], Xin Ou[e], Tadatomo Suga[a,d]

[a] Department of Precision Engineering, School of Engineering, The University of Tokyo, Bunkyo, Tokyo 113-8656, Japan
[b] Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China
[c] University of Chinese Academy of Sciences, Beijing 100049, China
[d] Kunshan Branch, Institute of Microelectronics of Chinese Academy of Sciences, Kunshan, Jiangsu 215347, China
[e] State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China

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ABSTRACT

Integration of Ga_2O_3 on SiC substrate with a high thermal conductivity is one of the promising solutions to reduce the self-heating of Ga_2O_3 devices. Direct wafer bonding of Ga_2O_3–SiC at room temperature was achieved by surface activated bonding (SAB) using a Si-containing Ar ion beam. An average bonding energy of ~2.31 J/m^2 was achieved. Both the structure and the composition of the interface were investigated to understand the bonding mechanism. According to the interface analysis, a ~2.2 nm amorphous SiC layer and a ~1.8 nm amorphous β-Ga_2O_3 layer originating from the ion beam bombardment for surface activation were found at the interface. A slight diffusion at the interface might already happen at room temperature, which should contribute to the strong bonding. To confirm the diffusion at a low temperature and investigate the possible interfacial variation during device operation, an annealing process was carried out at 473 K. The same analysis was applied on the annealed bonding interface. The interfacial layer shrank by ~0.5 nm after annealing. The further diffusion of Ga and Si at the interface caused by the annealing was confirmed. Besides, the position of the Ar count peak inside the amorphous Ga_2O_3 layer shifted by ~0.5 nm toward SiC.

1. Introduction

Power devices are the key components in the electric vehicles, generators, trains and other important fields. Recently, beta-phase gallium oxide (β-Ga_2O_3), which is a wide-bandgap semiconductor material, has attracted extensive attention as the candidate for power devices due to its wide band gap (4.8–4.9 eV) and high breakdown field (theoretically ~8 MV/cm) [1–3]. Besides the electronic characteristics, β-Ga_2O_3 is also a material which can survive in harsh environments such as high temperature and acid or alkali environment (except some solutions such as HF and NaOH), and a material only responding to the wavelength below 280 nm which is a desired property for solar-blind photodetector [4,5]. These properties will extend the field of application for β-Ga_2O_3.

Up to now, a number of devices were made using β-Ga_2O_3, such as Schottky Barrier Diode (SBD), Field-Effect Transistor (FET), and photodetector for power devices or sensors [2,6]. However, compared to other semiconductor materials, β-Ga_2O_3 has a very low thermal conductivity (0.1–0.3 W/cm K), which will limit its potential for high-temperature applications [7].

A promising method to overcome this drawback is to combine β-Ga_2O_3 with high thermal conductivity substrates. Silicon carbide (SiC), which is a well-known wide band gap semiconductor material with a high thermal conductivity (4.9 W/cm K), shows potential as a heat dissipation substrate [8,9]. Stephen A. O. Russell et al. simulated a β-Ga_2O_3 FET on 4H-SiC, and the result showed that the self-heating is reduced by integrating β-Ga_2O_3 layer with SiC substrate due to its high thermal conductivity [10].

At the moment, the most common method to prepare β-Ga_2O_3 on SiC is hetero-epitaxial growth [7]. However, a SiC substrate with a high quality is always necessary to get a high quality epitaxial Ga_2O_3 layer, which is quite expensive [10]. Moreover, the process often requires high temperature, which decreases the integration compatibility [7]. Recently, a so-called scotch tape method has been employed to transfer the Ga_2O_3 nano-belt for device fabrication of photoconductors or FET [11–13]. This method is good to fabricate stand-alone device, but barely achieved large scale transfer.

Considering the requirements of large scale transfer of high quality Ga_2O_3 layer and low temperature integration, wafer bonding between β-Ga_2O_3 and SiC at a low temperature seems to be an appropriate

* Corresponding author.
E-mail address: mu.fengwen@su.t.u-tokyo.ac.jp (F. Mu).

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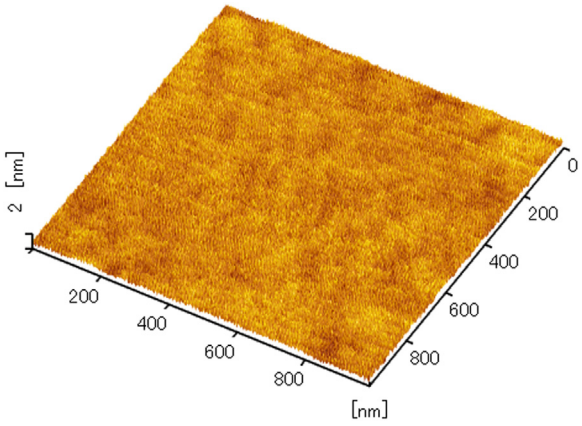

Fig. 1. DFM image of the Ga_2O_3 ($\bar{2}01$) surface.

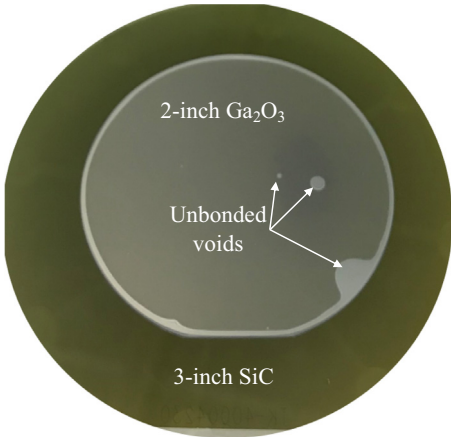

Fig. 2. The bonded Ga_2O_3-SiC wafer at room temperature by SAB method.

solution. Up to now, the research of wafer bonding between β-Ga_2O_3 and high thermal conductivity materials has not been reported.

In this study, we achieved wafer bonding of SiC and β-Ga_2O_3 at room temperature using a surface activated bonding (SAB) method, in which a Si-containing Ar ion beam was used to activate the two surfaces prior to bonding in an ultra-high vacuum (UHV) environment [14,15].

2. Experimental

The SiC wafers used are n-type, 3-in., 4° off-axis 4H-SiC with a thickness of ~360 μm. The Si-face of 4H-SiC wafer was used as the bonding surface. The Ga_2O_3 samples used are 2-in. β-Ga_2O_3 ($\bar{2}01$) wafer with a thickness ~680 μm, which are commercialized products from Tamura Corp. All of the bonding surfaces were polished by chemical mechanical polishing (CMP). Their root-mean-square (RMS) roughness was measured by dynamic force microscopy (DFM; Hitachi High Tech Science NanoNavi/L-trace II). The RMS surface roughness of SiC Si-face and Ga_2O_3 ($\bar{2}01$) surface was ~0.30 nm and ~0.27 nm, respectively. The DFM image of Ga_2O_3 ($\bar{2}01$) surface is shown in Fig. 1.

The bonding process was performed in our UHV-bonding machine, which consists of a load-lock chamber and a processing-bonding chamber. A Si-containing Ar ion beam was set for surface activation in the processing-bonding chamber. After surface activation by the ion beam, the samples were bonded directly at room temperature under 5 MPa for 180 s. The other bonding parameters have been described in a previous publication [15]. After bonding, the bonding energy (γ), which is the fracture energy of bonding interface, was evaluated by the "crack-opening" method and calculated by the following equation [16].

$$\gamma = \frac{3t_b^2 E_1 t_{w1}^3 E_2 t_{w2}^3}{16L^4(E_1 t_{w1}^3 + E_2 t_{w2}^3)} \quad (1)$$

where E_1 and E_2 are the Young's moduli of SiC (530 GPa) and Ga_2O_3 (230 GPa), t_{w1} and t_{w2} are the thickness of two bonded wafers, t_b is the thickness of the blade, and L is the crack length. This measurement was carried out at room temperature in air at a relative humidity (RH) of ~36.5%. To make the bonding mechanism clear, the bonding interface was investigated by an aberration corrected scanning transmission electron microscopy (STEM; Hitachi HD2700 STEM) and energy dispersive spectroscopy (EDS, Bruker Quantax). To confirm the diffusion at a low temperature and check the interface changes at an assumed operation temperature of Ga_2O_3 devices, the bonded specimen was annealed at 473 K for 72 h in air, followed by the same interface analysis.

3. Results and discussion

Fig. 2 is the photo of the bonded Ga_2O_3-SiC wafer. It can be seen that the wafer was almost completely bonded, except a few voids and the edge exclusion area. The bonding energy is in the range of 2.16–2.60 J/m^2 with an average of ~2.31 J/m^2. Fig. 3(a) and (b) show the bright field (BF) STEM images of the bonding interface before and after annealing, respectively. For the bonding interface without annealing, as shown in Fig. 3(a), there are two amorphous layers at the interface, which should be one amorphous SiC layer and one amorphous Ga_2O_3 layer. These amorphous layers were caused by ion beam bombardment. The thickness of the amorphous SiC and amorphous Ga_2O_3 are ~2.2 nm and ~1.8 nm, respectively. In Fig. 3(b), the bonding interface after annealing at 473 K also consists of one amorphous SiC layer and one amorphous Ga_2O_3 layer. The thickness of the amorphous SiC is still ~2.2 nm, however, the amorphous Ga_2O_3 layer became ~0.5 nm thinner. One reasonable explanation is the interfacial layer shrank due to interfacial diffusion during annealing.

The high-angle annular dark-field (HAADF) STEM image of the bonding interface before and after annealing are shown in Fig. 4(a) and (b), respectively. The Ga_2O_3 is brighter than SiC because the atomic number of Ga is much higher than that of Si and C. The bright part in the interfacial layer represents the existence of Ga. As shown in Fig. 4(a), there is one dark layer and one bright layer at the interface with different contrasts from both of SiC and Ga_2O_3 substrate. The Ga is distributed in the bright interfacial layer close to Ga_2O_3 substrate, which has a thickness of ~1.8–1.9 nm. This means the dark and the bright interfacial layer in Fig. 4(a) correspond to the amorphous SiC layer and the amorphous Ga_2O_3 layer shown in Fig. 3(a), respectively. In addition, the interface between the two interfacial layers in Fig. 4(a) is not very sharp, indicating that there might be a slight diffusion between the amorphous Ga_2O_3 and the amorphous SiC, even at room temperature, which should contribute to the strong bonding we achieved. After annealing, the interface between the two interfacial layers became even more indistinct, which means the diffusion could further happen at the interface during a low temperature annealing. Besides, the dark interfacial layer after annealing became thinner compared to that before annealing. This should also be caused by the interfacial diffusion of Ga toward SiC during annealing.

To confirm the above analysis, especially the diffusion at the interface during annealing, the composition of the interface before and after annealing was analyzed by the line-scanning of EDS. The distribution profiles of Ar, Ga, Si, and O at the interface before and after annealing were compared in Fig. 5(a), (b), (c) and (d), respectively. Since there is a lot carbon contamination during sample preparation, C was not taken in consideration.

As shown in Fig. 5(a), there are two Ar count peaks at the interface for both of the samples before and after annealing. One of the peaks is located in the amorphous Ga_2O_3 and the other is located in the amorphous SiC. This is caused by the Ar implantation during the ion beam bombardment for surface activation. By comparing the position of the

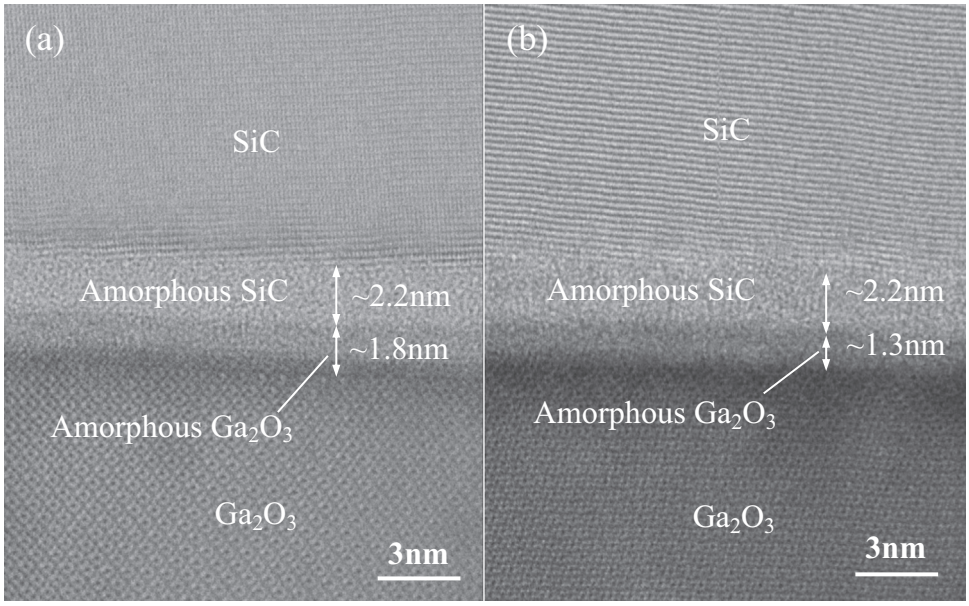

Fig. 3. BF STEM images of the Ga_2O_3-SiC bonding interface (a) before annealing (b) after annealing.

Ar count peaks before and after annealing, a very interesting phenomenon was found. The Ar count peak inside the amorphous Ga_2O_3 was shifted toward the SiC side by ~0.5 nm, which may be caused by the shrink of interfacial layer due to the diffusion during annealing. From the dash-lined rectangular area in Fig. 5(b) and (c), it can be clearly confirmed that both Ga and Si diffused towards SiC and Ga_2O_3, respectively, more than 2 nm during annealing. Besides the Si atoms introduced by Si-containing Ar ion beam, the Si atoms from amorphous SiC should also contribute to the diffusion during annealing. This could be confirmed by the none of clear turning point in the position range from −2 to 2 nm of the Si curve for the sample after annealing, which is different from that before annealing, as shown in Fig. 5(c). In accordance with the Fig. 5(d), the diffusion of oxygen during annealing has not happened.

4. Conclusions

In this study, the direct wafer bonding of SiC and β-Ga_2O_3 was successfully realized at room temperature by our SAB method using a Si-containing Ar ion beam. The two wafers were almost completely bonded with an average bonding energy of ~2.31 J/m^2. The interface bonded at room temperature was analyzed by STEM and EDS. A ~1.8 nm amorphous β-Ga_2O_3 layer and a ~2.2 nm amorphous SiC layer generated from ion beam bombardment prior to bonding was confirmed at the interface. A slight diffusion at the interface might already happen at room temperature. An annealing process was carried out at 473 K for 72 h to confirm the assumed low temperature interfacial diffusion and investigate the possible variation of the bonding interface during device operation. The further diffusion of Ga and Si at the interface caused by annealing was confirmed. The interfacial layer shrank by ~0.5 nm, which may be the reason of the position shift of the Ar count peak inside the amorphous Ga_2O_3 layer. The effect of the interfacial diffusion

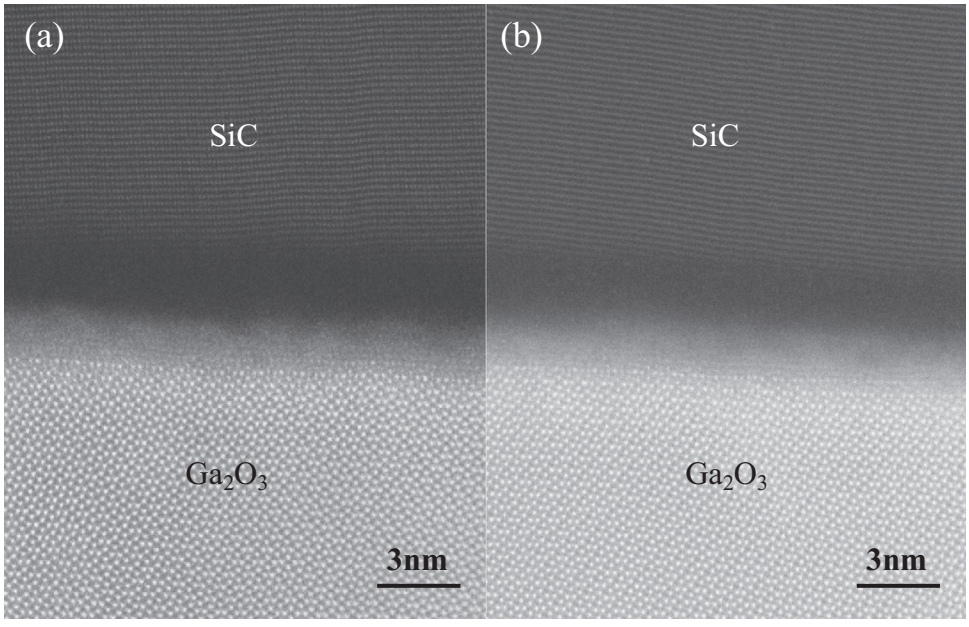

Fig. 4. HAADF STEM images of the Ga_2O_3-SiC bonding interface (a) before annealing (b) after annealing.

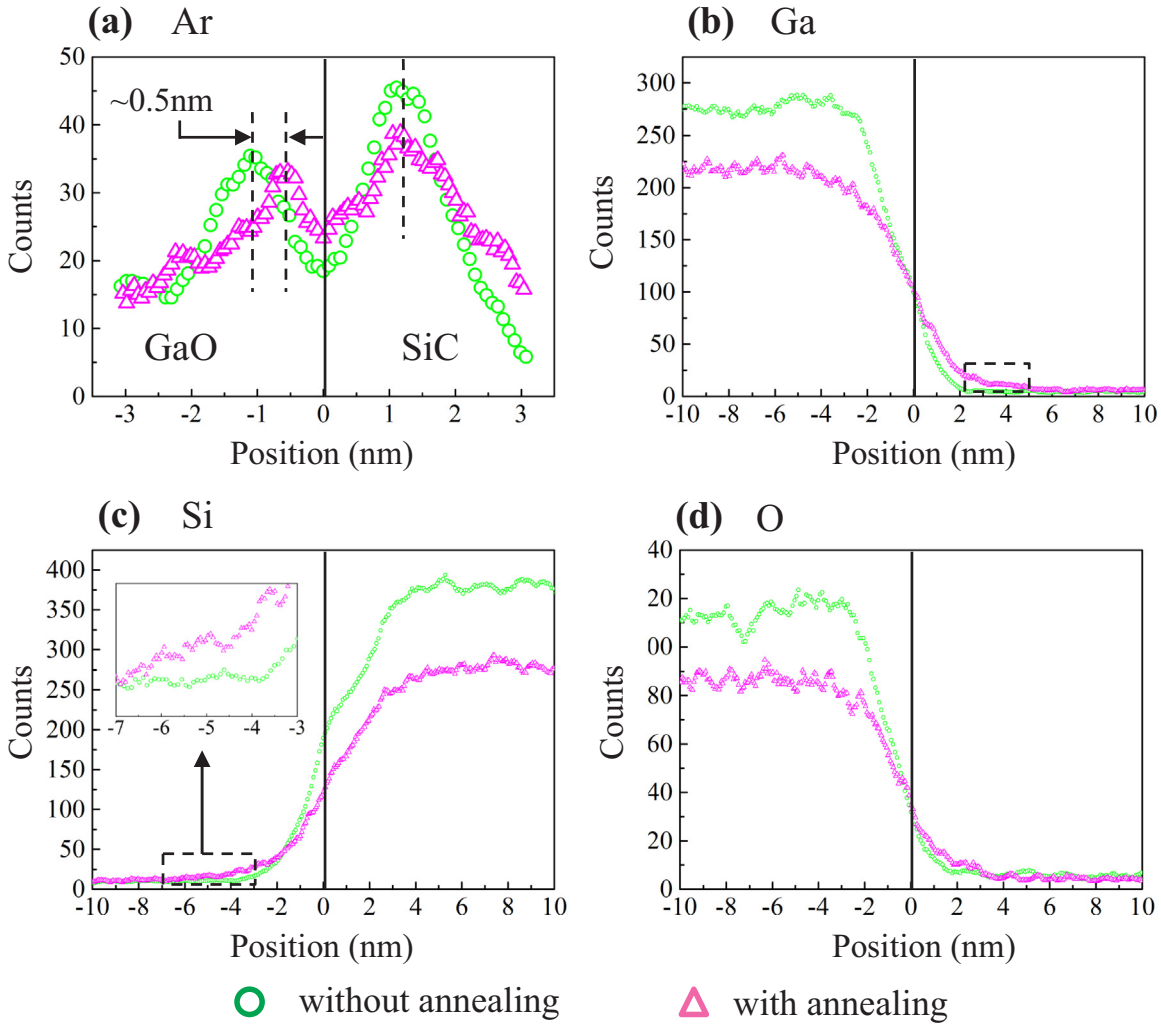

Fig. 5. The distribution profiles of (a) Ar, (b) Ga, (c) Si, and (d) O from EDS line-scanning across the bonding interface. The results of the interface without and with annealing are drawn using green circles and magenta triangles, respectively. The rectangular area of dash line in (b) and (c) helps to see the diffusion depth of Ga and Si. The inserted picture in (c) shows the magnification of the Si distribution profile in the rectangular area of dash line.

during annealing would be further evaluated depending on the specific applications. The integration of Ga_2O_3 and SiC via wafer bonding is expected to reduce the self-heating of Ga_2O_3 device at a low cost in the future.

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